

FIG. 1
PRIOR ART

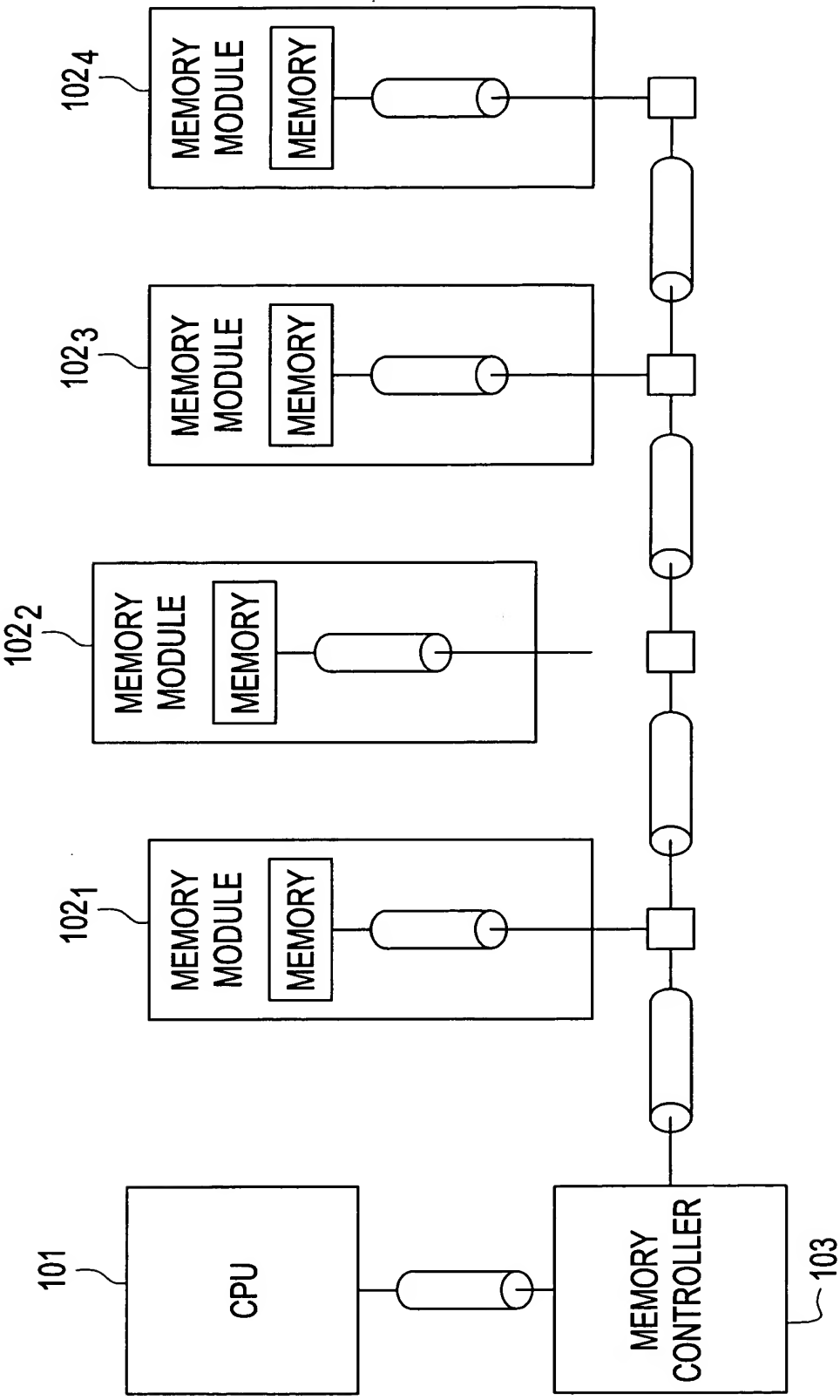


FIG. 2
PRIOR ART

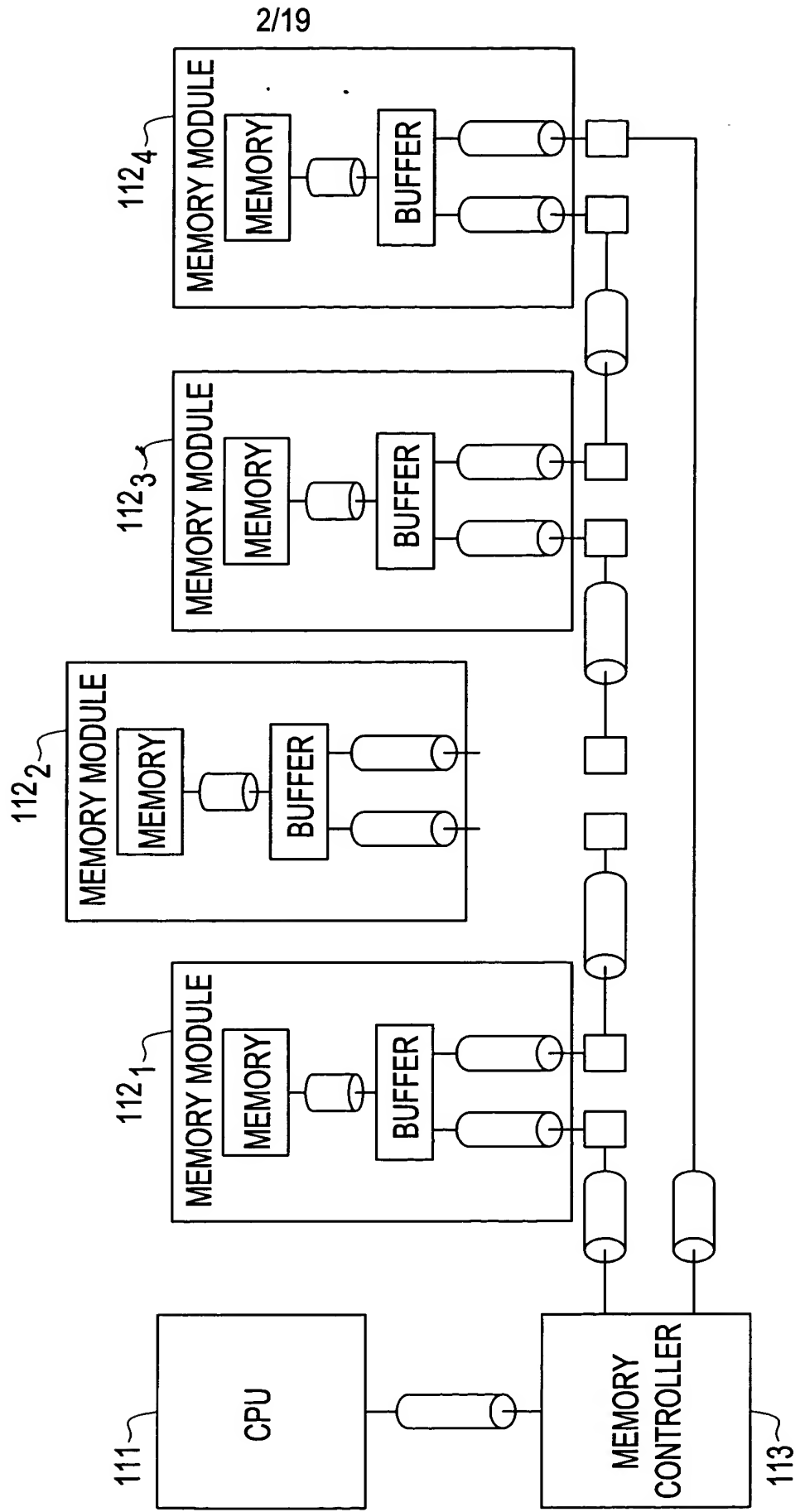


FIG. 3
PRIOR ART

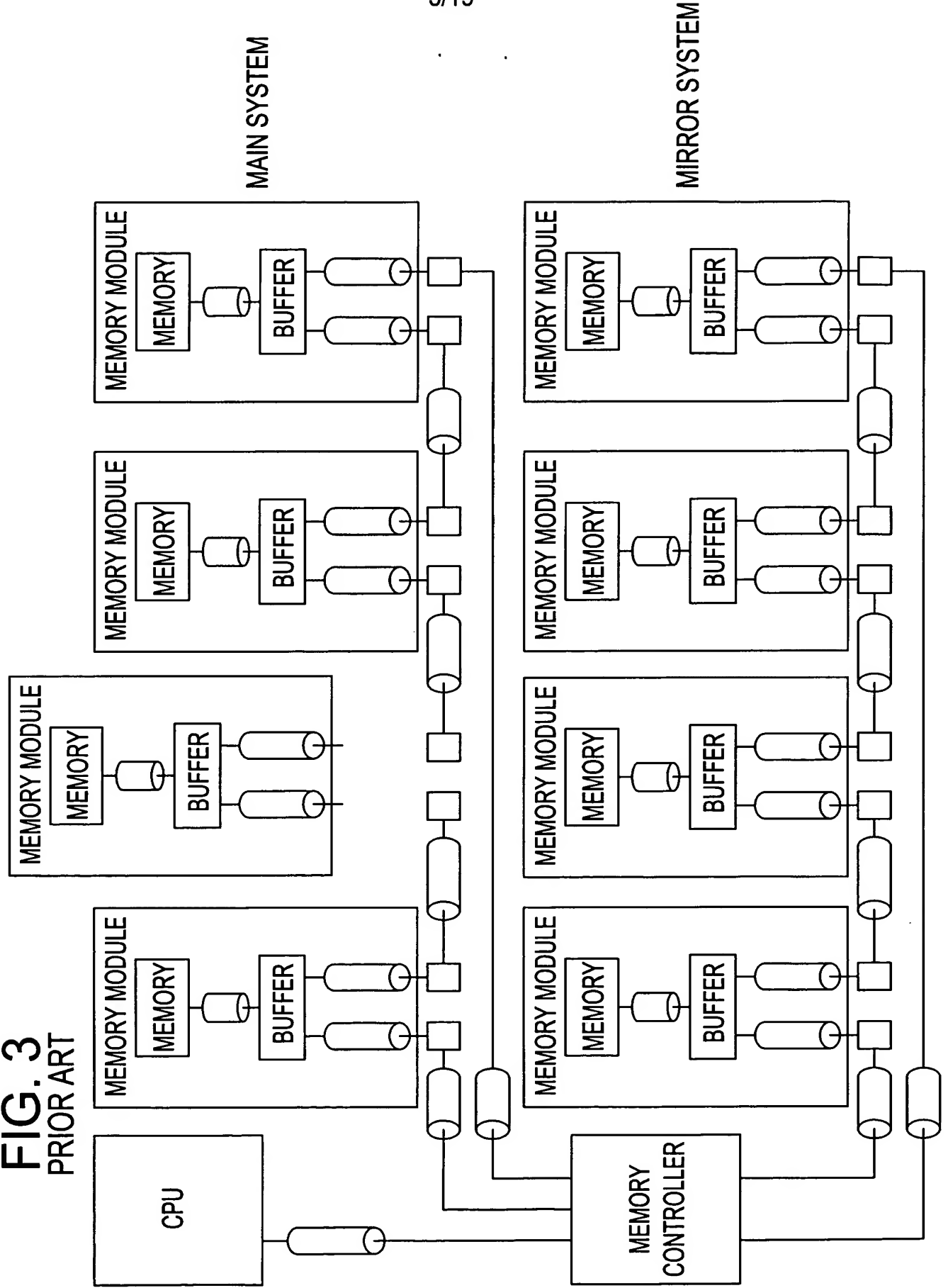


FIG. 4

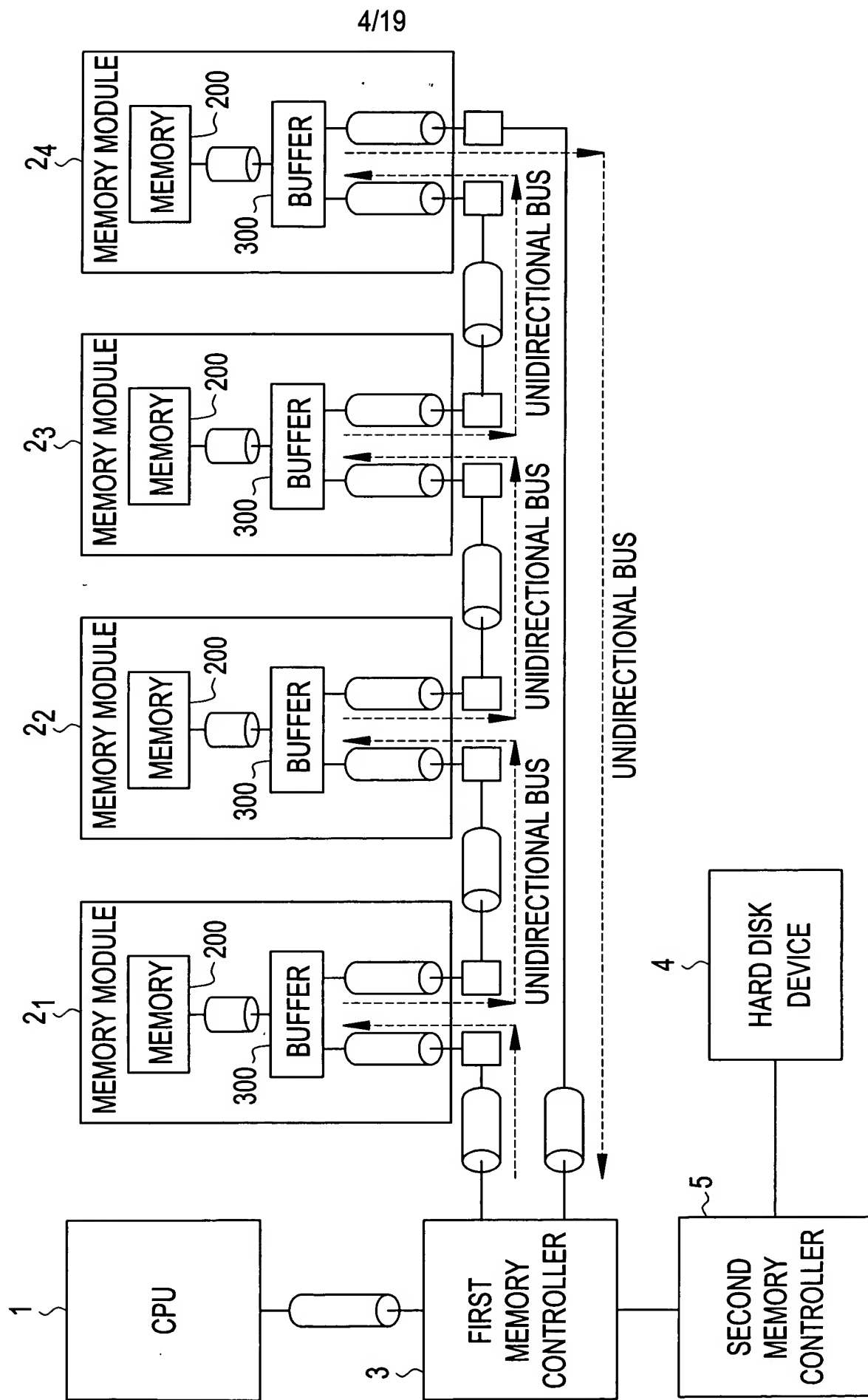


FIG. 5

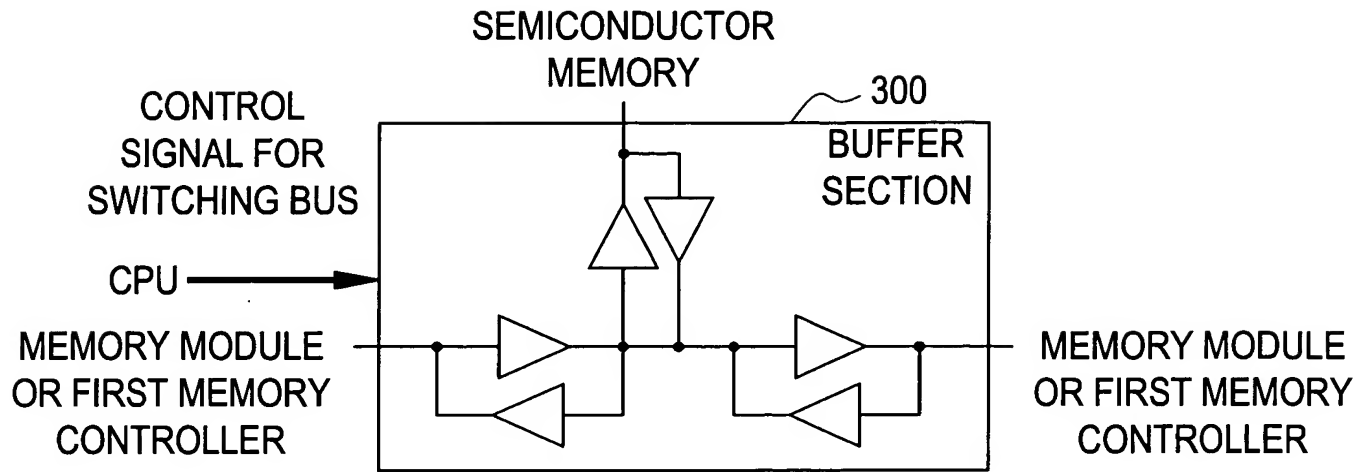


FIG. 6A

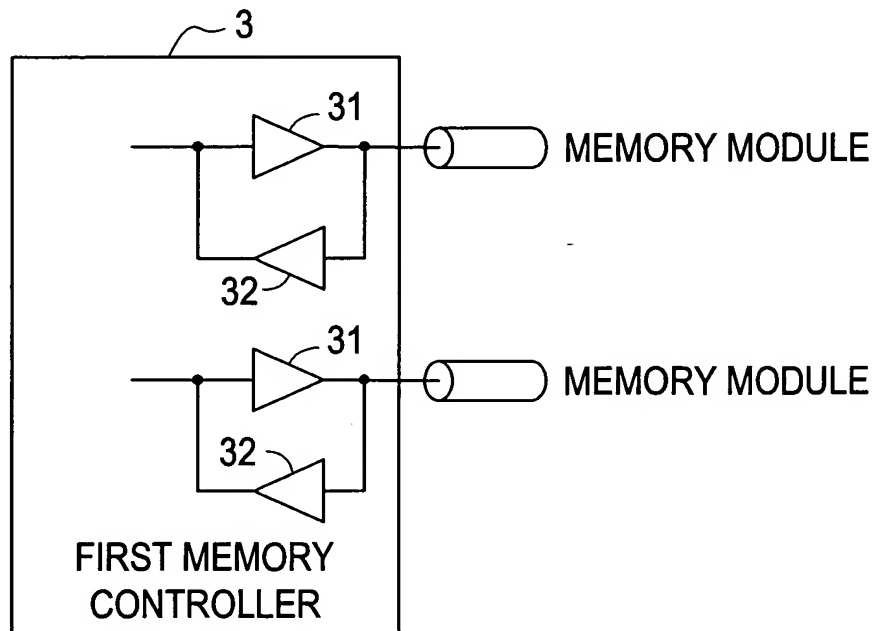


FIG. 6B

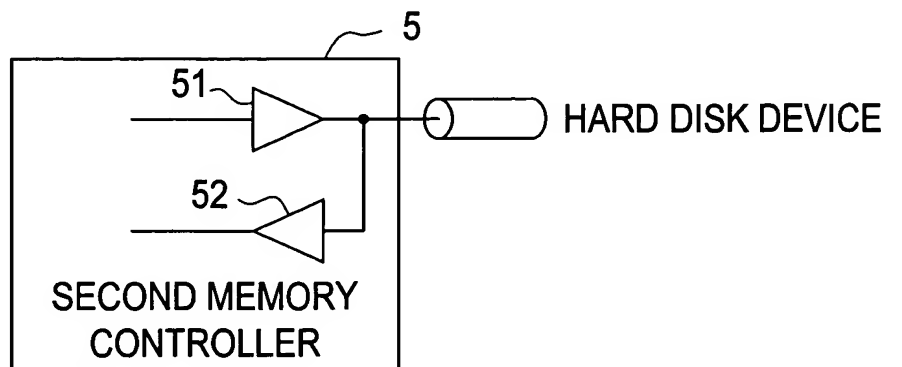


FIG. 7

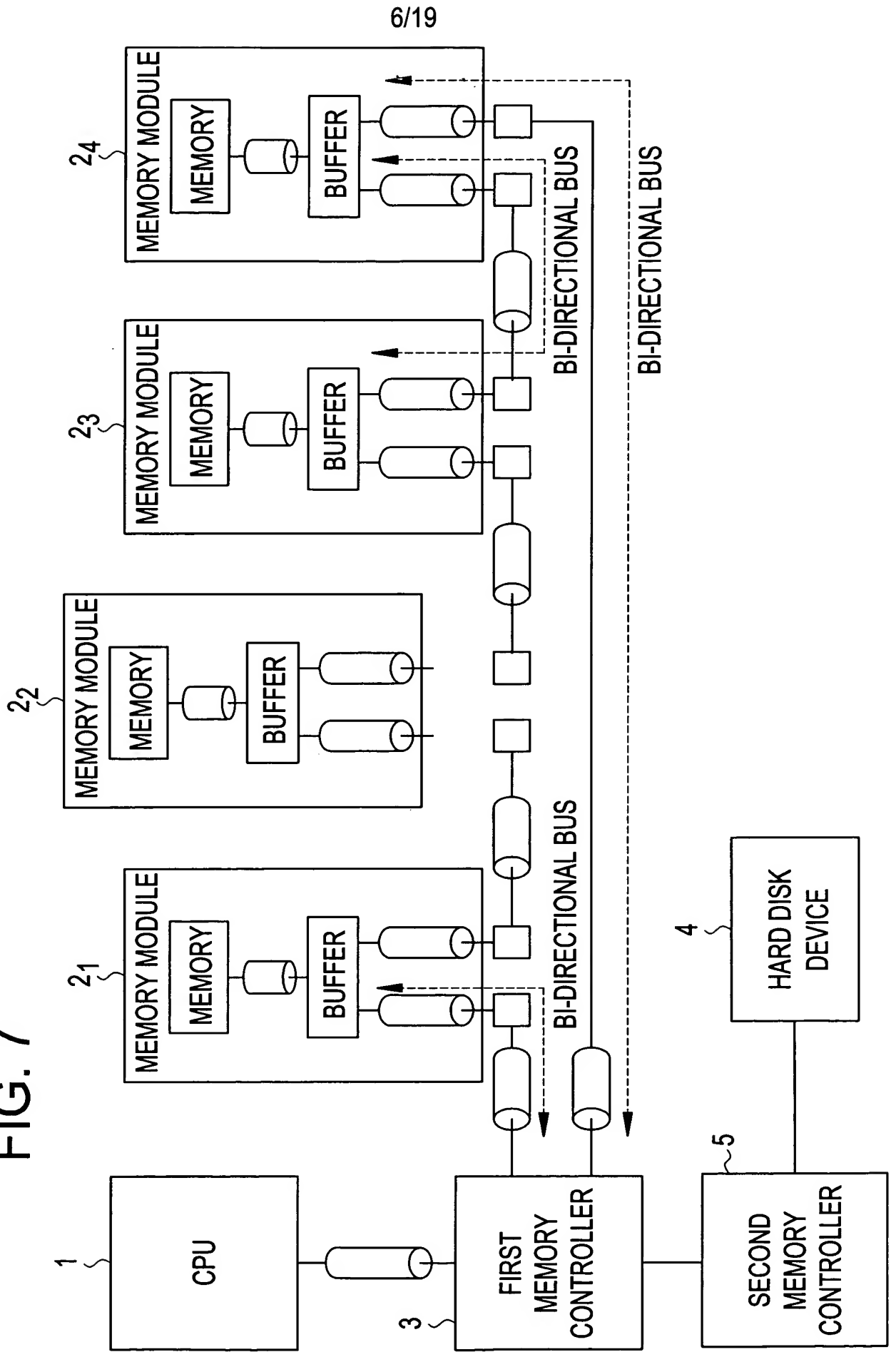


FIG. 8

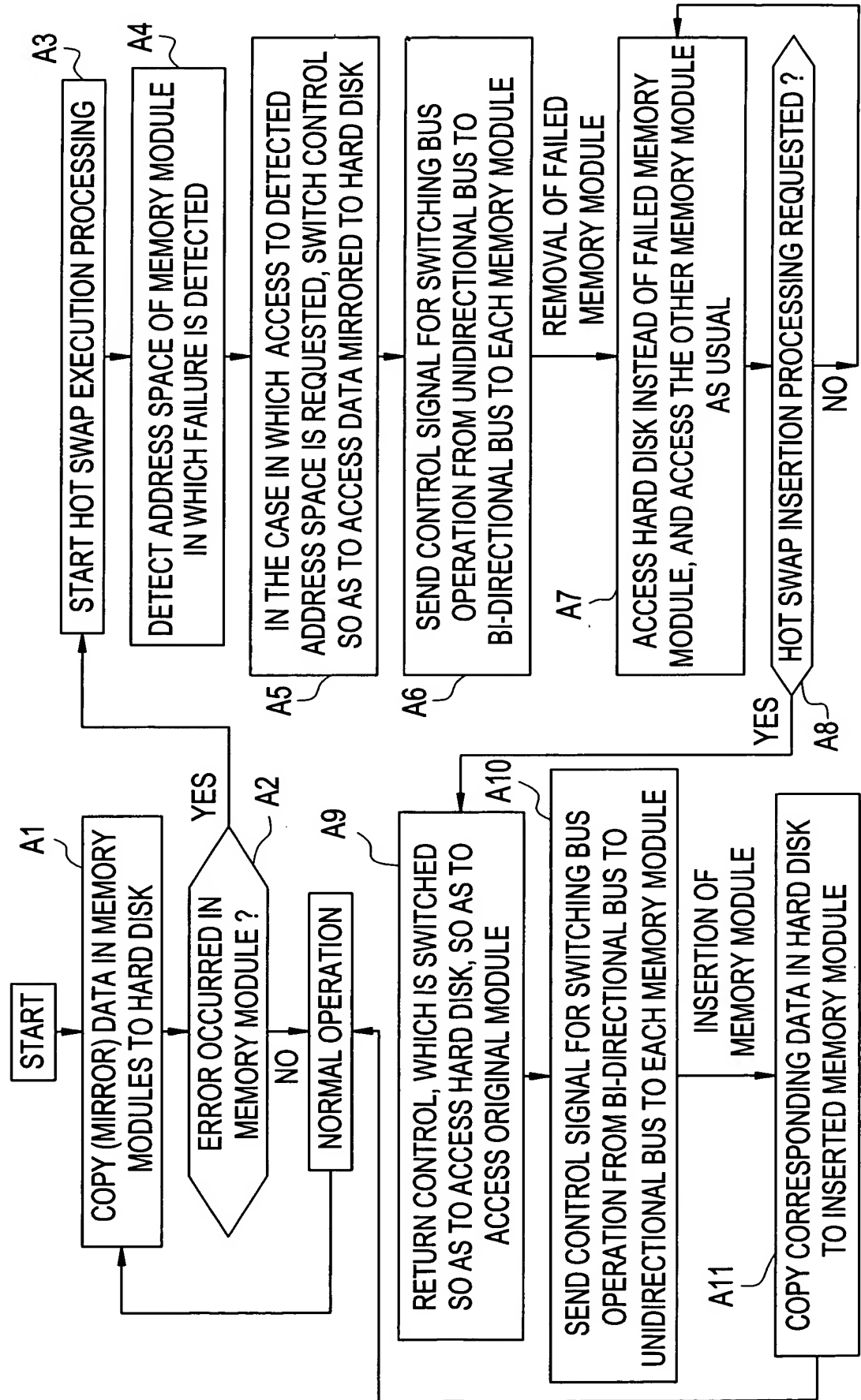


FIG. 9

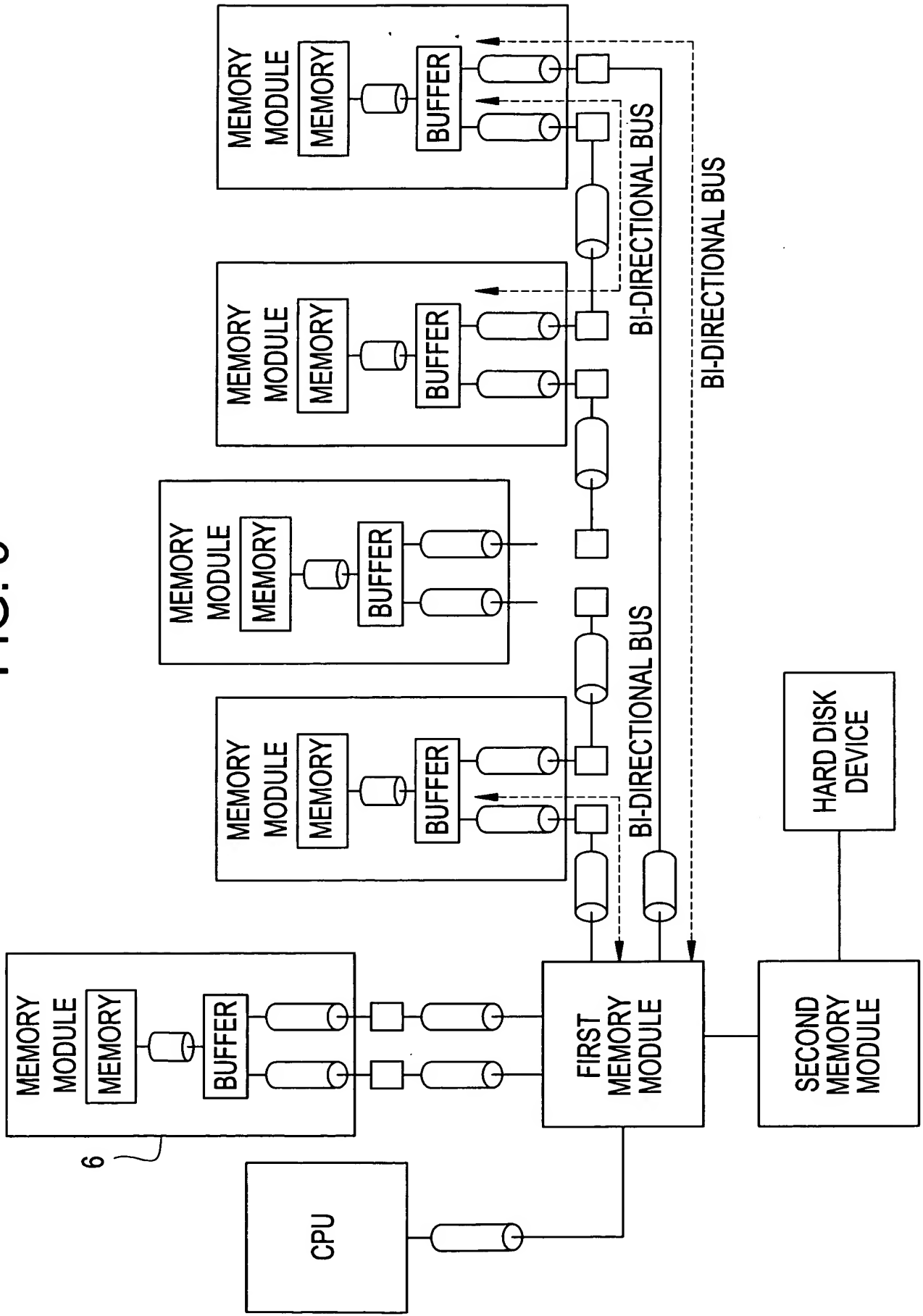


FIG. 10

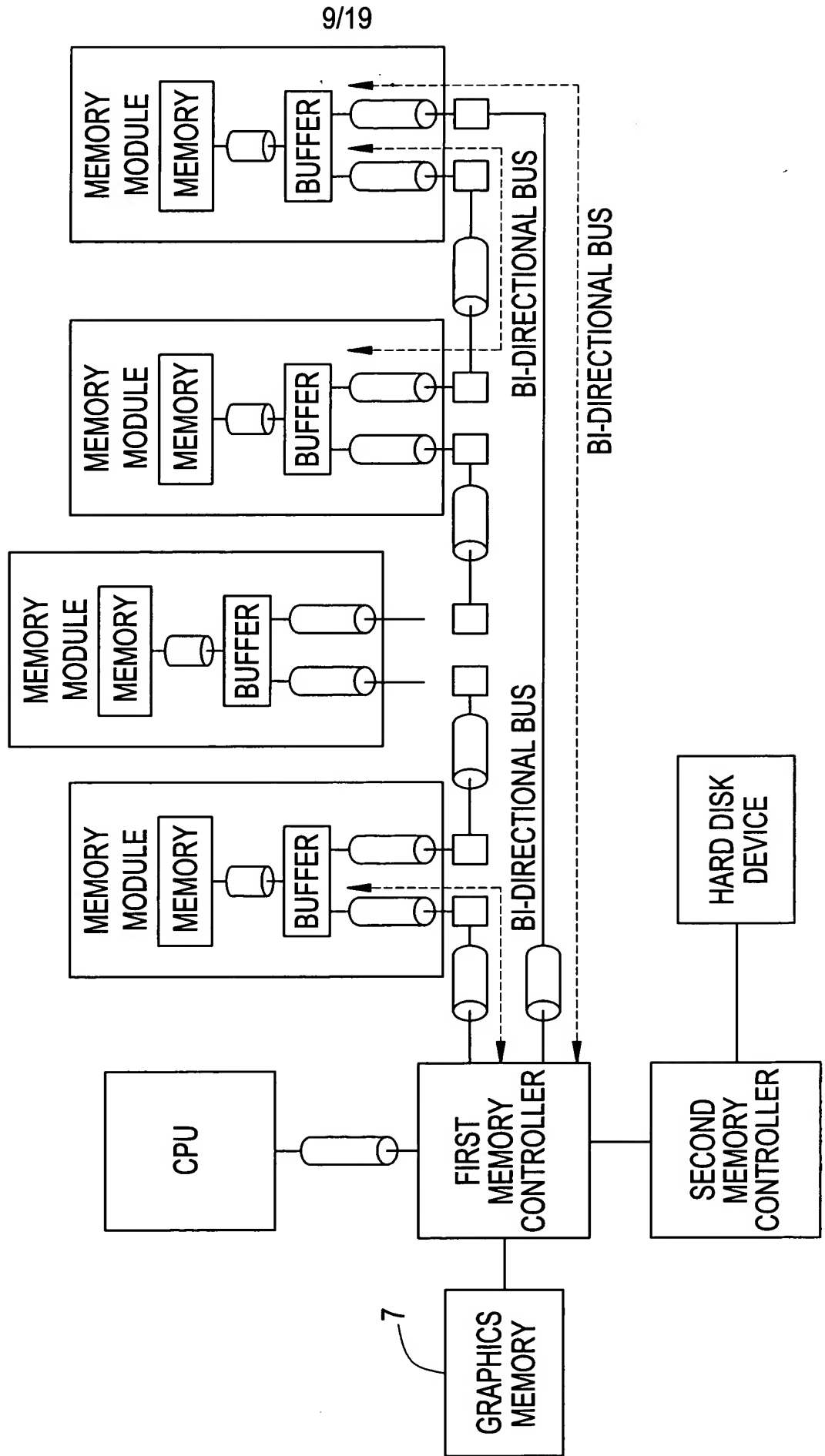


FIG. 11

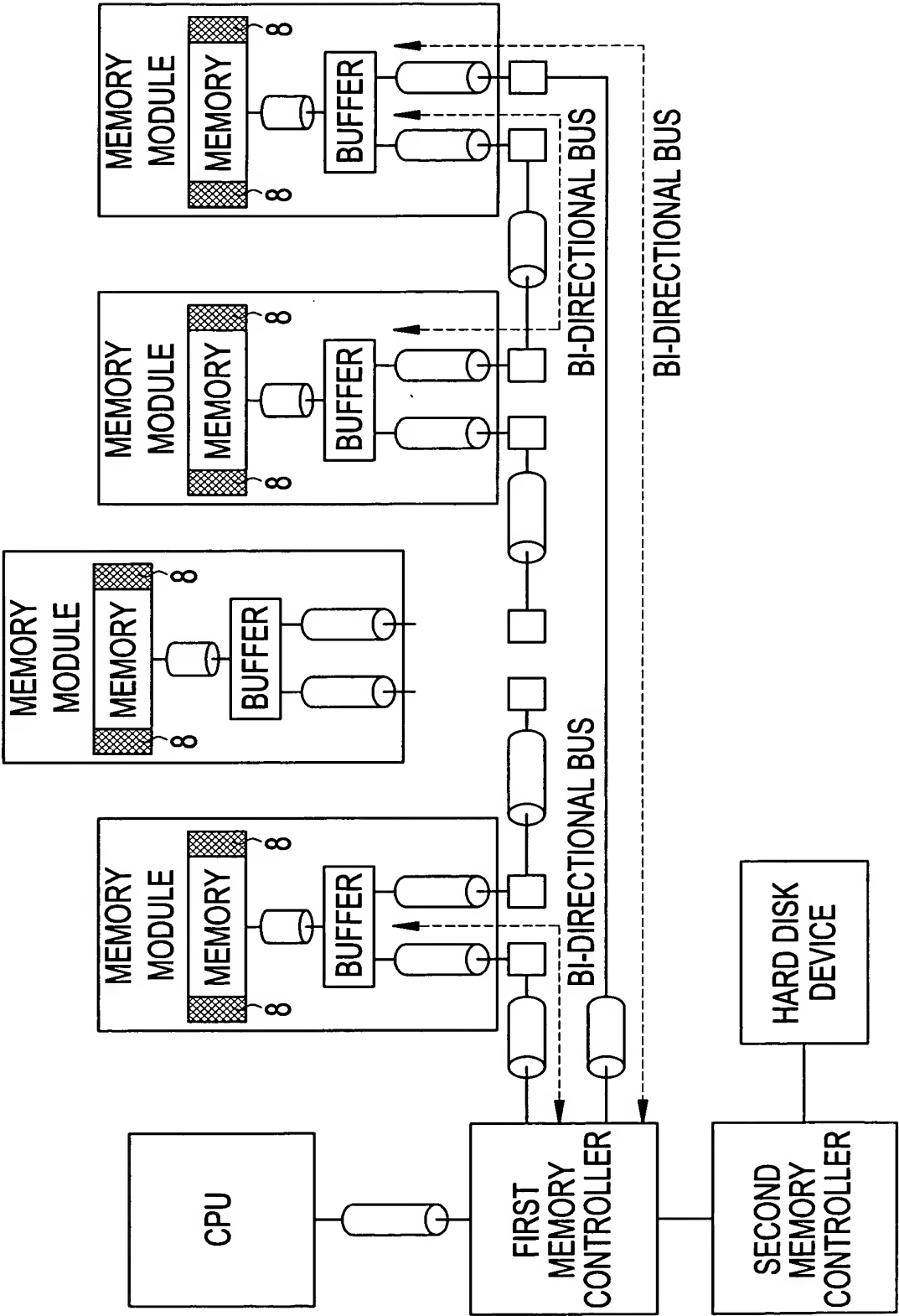


FIG. 12

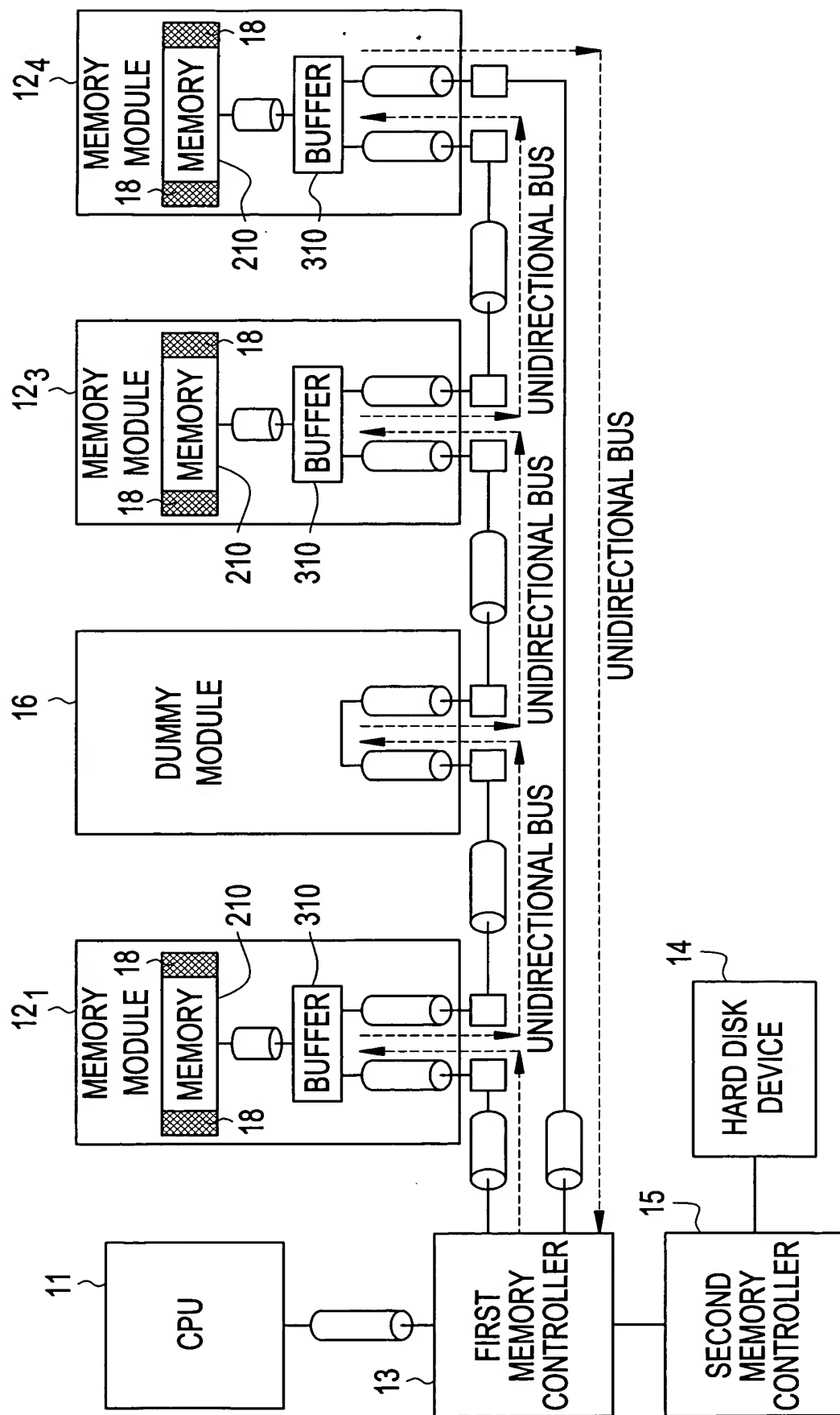


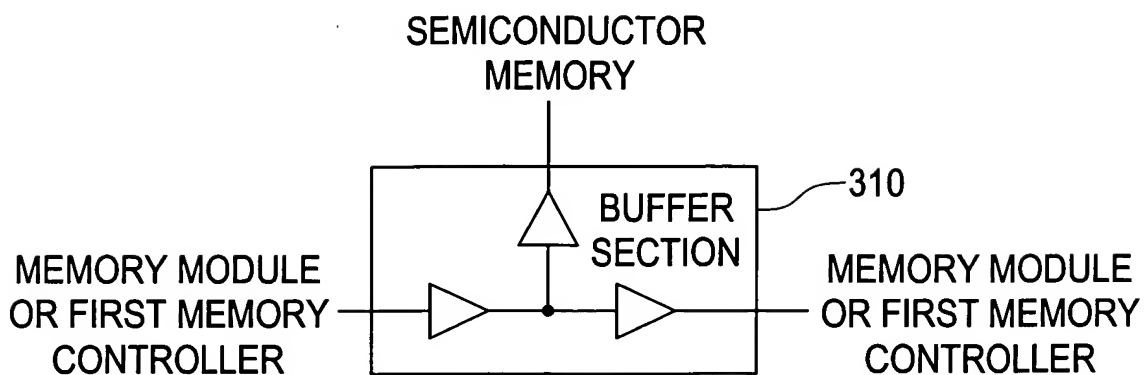
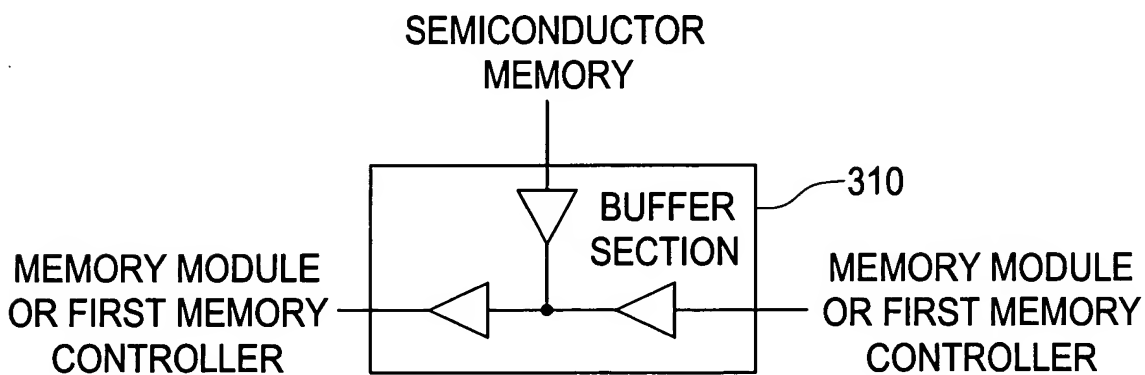
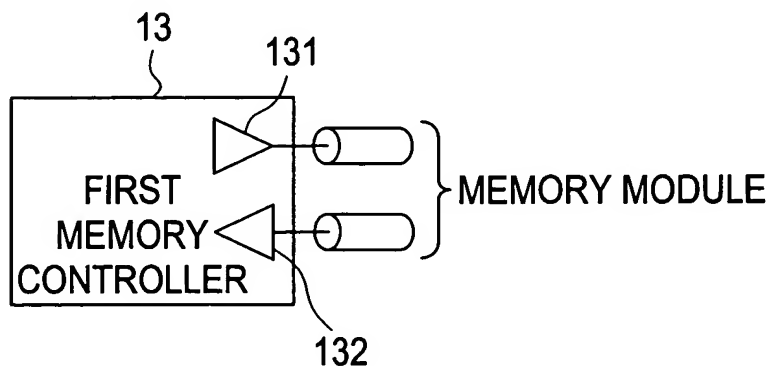
FIG. 13A**FIG. 13B****FIG. 14**

FIG. 15

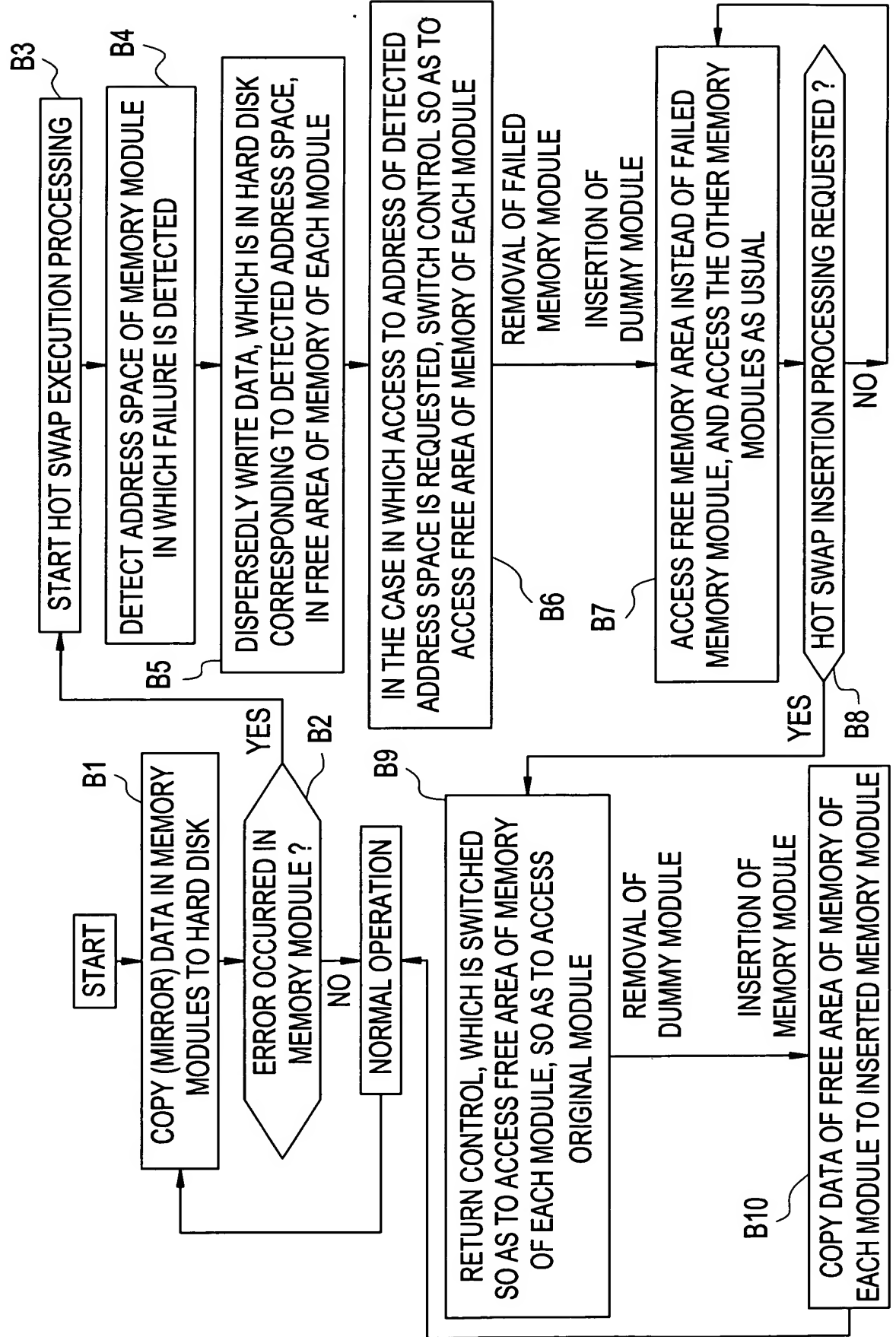


FIG. 16

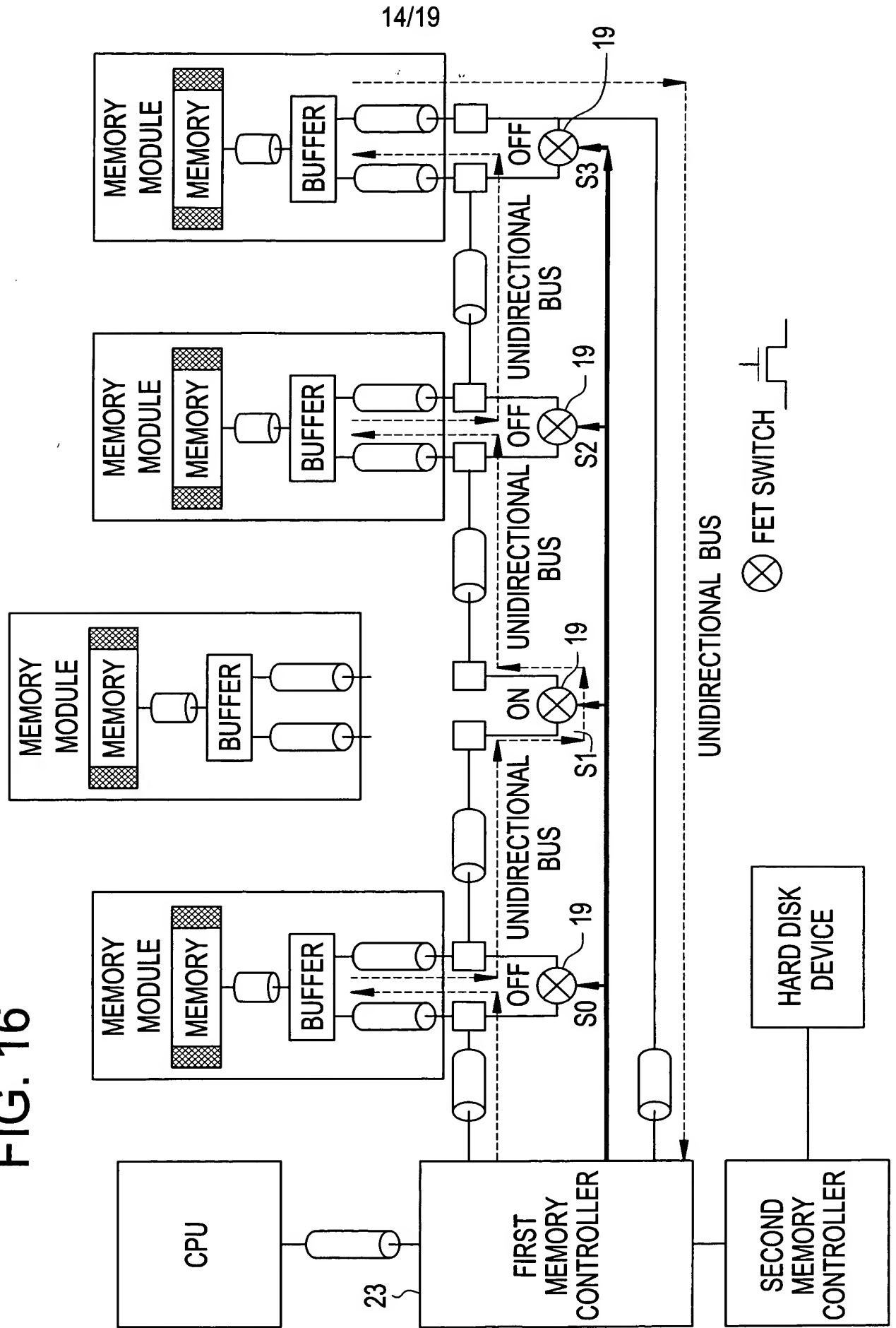
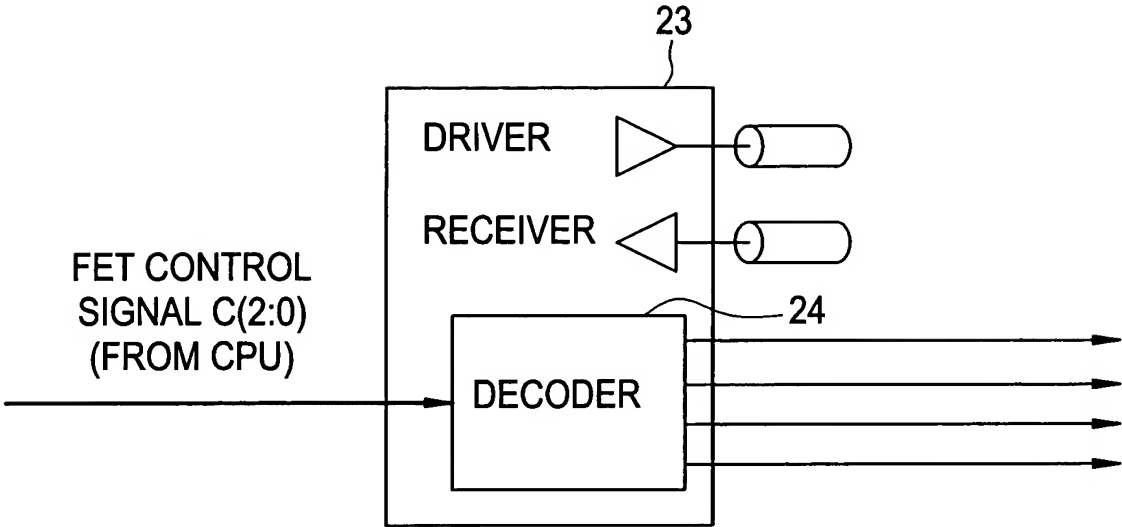


FIG. 17



FET CONTROL SIGNAL						
C2	C1	C0	S3	S2	S1	S0
H	L	L	L	L	L	L
L	L	L	L	L	L	H
L	L	H	L	L	H	L
L	H	L	L	H	L	L
L	H	H	H	L	L	L

L : FET SWITCH OFF
H : FET SWITCH ON

FIG. 18

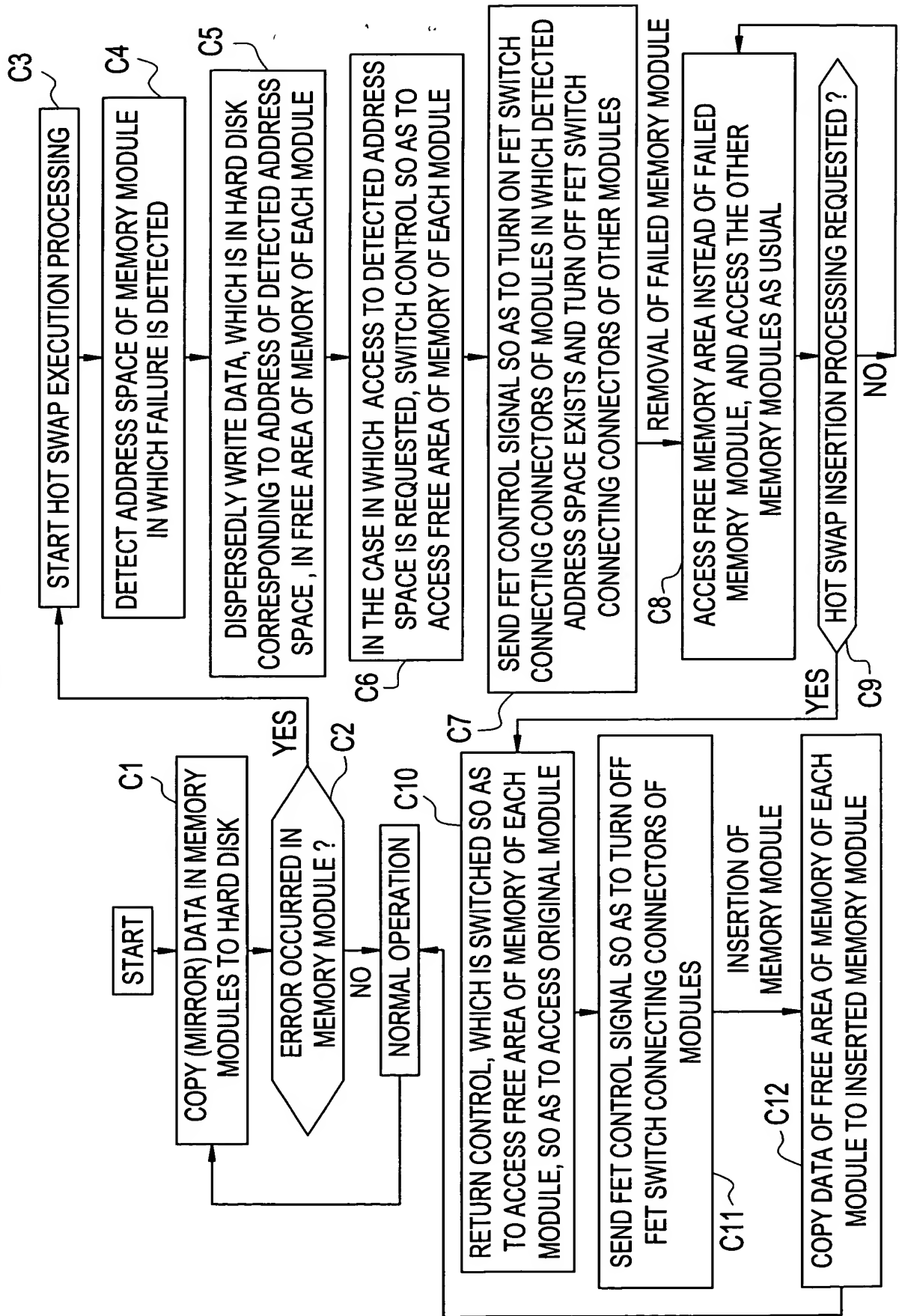


FIG. 19

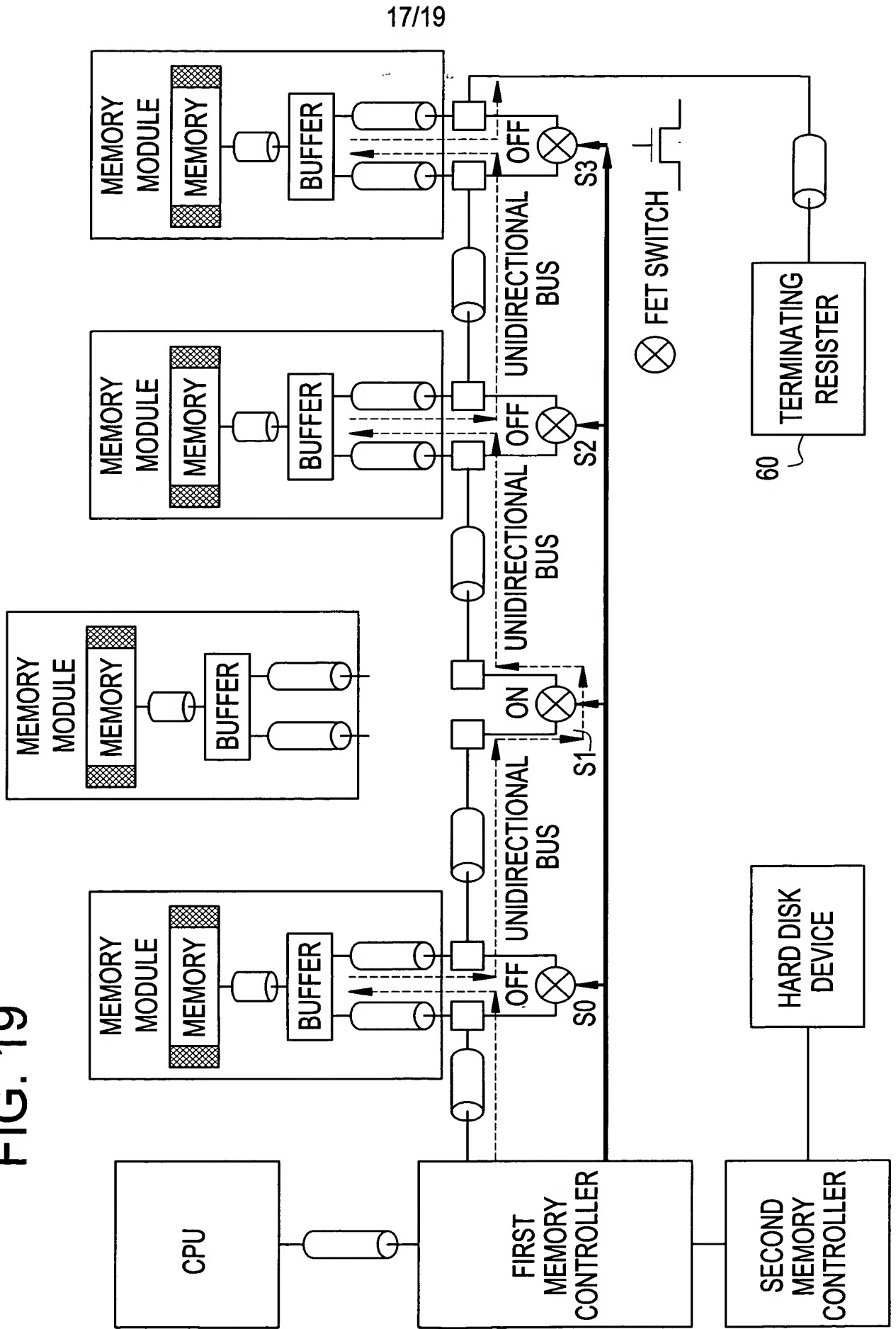


FIG. 20

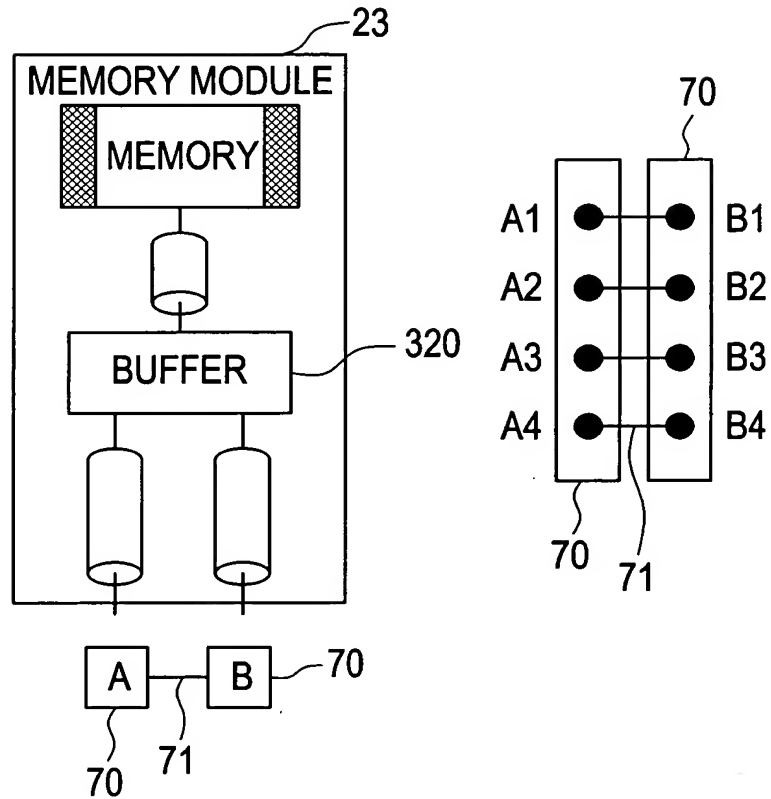


FIG. 21A

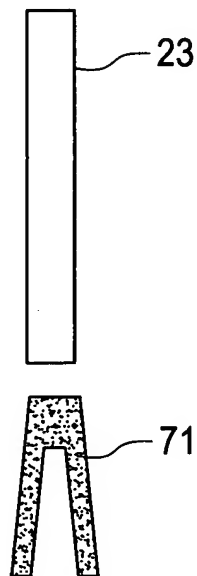


FIG. 21B

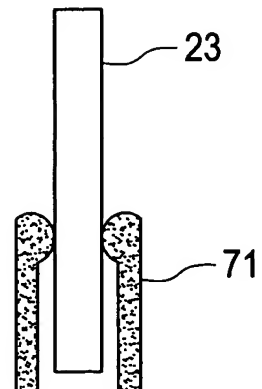


FIG. 22

